(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 379 709 B1**

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification : **23.08.95 Bulletin 95/34**

(51) Int. Cl.[6] : **G06F 7/22**, G06F 5/06, G06F 13/16

(21) Application number : **89123610.1**

(22) Date of filing : **21.12.89**

(54) **Single-fifo high speed combining switch.**

(30) Priority : **27.01.89 US 303699**

(43) Date of publication of application : **01.08.90 Bulletin 90/31**

(45) Publication of the grant of the patent : **23.08.95 Bulletin 95/34**

(84) Designated Contracting States : **DE FR GB**

(56) References cited :
US-A- 4 750 154
INTERNATIONAL SYMPOSIUM ON VLSI TECHNOLOGY SYSTEMS AND APPLICATIONS 1987, NEW YORK, US pages 349-353; Y. HSU ET AL.: 'Designing of a combining network for the RP3 project.'

(73) Proprietor : **International Business Machines Corporation**
Old Orchard Road
Armonk, N.Y. 10504 (US)

(72) Inventor : **Hsu, Yarsun**
45 Deerfield Lane South
Pleasantville NY 10570 (US)

(74) Representative : **Schäfer, Wolfgang, Dipl.-Ing. et al**
IBM Deutschland Informationssysteme GmbH
Patentwesen und Urheberrecht
D-70548 Stuttgart (DE)

EP 0 379 709 B1

Description

SINGLE-FIFO HIGH SPEED COMBINING SWITCH

This invention relates generally to data switching apparatus and, in particular, to a high speed data combining switch which employs, for each half, a single first-in/first-out (FIFO) buffer having an output coupled to a switch output port.

Some multi-processor data processing systems include a number of data processors coupled to a number of memory modules through an interconnection network. The interconnection network may employ an Omega-type switch which includes log(n) stages of n/2 two-by-two switches, where n represents the number of ports being serviced by the switch. One type of switch is known as a combining switch which is used to combine multiple messages which are addressed to the same memory location in order to reduce the number of accesses to that memory location. By combining messages the effects of "hot spot" loading are reduced and the bandwidth of the interconnection network is increased. A decombining switch is subsequently employed to "decombine" responses from memory modules and transmit the responses back to the processors.

Fig. 1 illustrates a conventional 2 X 2 combining switch 1 comprised of two substantially identical halves. For convenience only one half of the switch will be discussed, the corresponding structure in the other switch half being designated by a primed reference number. Each switch half includes two FIFO register files, one being known as a Chute FIFO 2 and the other being known as a Queue FIFO 3. The Chute and Queue FIFOs each have an equal number of storage locations and are employed to store messages before transmission to the network of memory modules (not shown). Typically, if there are no contentions or congestions at the switch output port 4 and the Queue 3 is empty, incoming processor messages from input ports I and J are routed directly to the output port 4 via a multiplexer 5. If the Queue 3 is not empty the incoming message is temporarily stored in an input register 6 and compared by a comparator 7 to all existing messages in the Queue to determine if the incoming message is directed to a memory location already associated with a queued message. If a match is not found the incoming registered message is stored in the next available location within the Queue FIFO 3. If a match is detected by the comparator 7 the incoming message is stored instead in the Chute FIFO 2 at a location corresponding to the storage location of the matched message in the Queue 3. Subsequently both the Chute and Queue messages are directed to an arithmetic logic unit (ALU) 8, via ALU input registers 9a and 9b, to combine and generate a single message. Information required for decombining the message on its return from the memory module is sent to a Wait Buffer in an associated decombining switch (not shown).

One significant disadvantage of such conventional combining switches is that the Chute FIFO register file occupies a significant portion of available integrated circuit area. For example, it can be shown that the Chute FIFO 2 can occupy thirty six percent of the data path area as compared to approximately forty five percent for the Queue and ten percent for the ALU. This significant area requirement, and the associated power requirement, for the Chute is especially disadvantageous if the majority of messages sent through the network are not combinable, resulting in only infrequent use of the Chute FIFO.

Another significant disadvantage of such conventional combining switches is that all output from the Queue, whether or not there is a corresponding entry in the Chute, is directed through the ALU. Thus, some finite amount of time is required for the message to pass through the ALU even for those messages which are not combined.

Typically an interconnection network is comprised of a plurality of 2 X 2 combining switches, such as an 8 X 8 network. It can therefore be appreciated that an improved packing density, higher speed and reduced power consumption of each of the 2 x 2 switches would result in an overall improvement in network performance.

It is therefore one object of the invention to provide a combining switch which operates at a higher speed than conventional combining switches.

It is another object of the invention to provide a combining switch which, for each switch half, includes only a Queue FIFO register and which directs messages directly from the Queue FIFO to the switch output port.

It is still another object of the invention to provide a combining switch which has a significant reduction in required integrated circuit surface area, which requires less operating power, and which operates at a higher speed than conventional combining switches.

The foregoing problems are overcome and the objects of the invention are realized by a data switching apparatus as defined in claim 1, specifically a combining switch having two halves, each of which includes an input port, an output port, a Queue FIFO, a comparator and an ALU. The input port receives data such as messages from data processors and directs incoming messages, if the output port is not busy and the Queue FIFO is empty, directly to the output port for transmission. If the output port is busy and the Queue FIFO is empty the incoming message is routed to the Queue FIFO for storage. If the Queue FIFO is not empty the incoming message is first compared by the comparator to all existing messages stored in the Queue FIFO to determine if the incoming message is destined for transmission to a memory location which already has a queued message. If no match is deter-

mined by the comparator the incoming message is routed to the Queue FIFO for storage. If the comparator determines that the destination location and typically also the operation type of an incoming message matches that of a message already stored in the Queue FIFO both the incoming message and the queued, matching message are applied to the message combining ALU. The ALU generates a combined message which is stored at the same Queue FIFO location as the queued message which generated the comparison match with the incoming message.

In accordance with a method of the invention as defined in claim 9, there is disclosed a method of operating a message combining switch in a data processing system of the type which includes a plurality of data processors which are coupled to a plurality of memory locations through a switching network, the data processors generating messages relative to identified ones of the memory locations. The message combining switch includes two halves each of which has a message storage unit, an input port and an output port. The method includes the steps of receiving a message from the input port and, if the message storage unit has at least one message stored within, comparing an identification of a memory location and an operation type associated with the received message to the identification of memory locations and operation types associated with messages stored in the message storage unit. If the memory location identification and operation type associated with one of the stored messages is determined to be equal to the memory location identification and operation type associated with the received message the method further includes the steps of combining the received message and the stored message to generate a combined message and replacing the stored message with the combined message.

The above set forth and other features of the invention will be made more apparent in the ensuing Detailed Description of the Invention when read in conjunction with the attached Drawing, wherein:

Fig. 1 is a simplified block diagram of a forward path of a 2 X 2 combining switch of the prior art having both Queue and Chute FIFO registers and ALUs through which all output of the Queue FIFOs are directed; and

Fig. 2 is a simplified block diagram of forward path of a 2 X 2 combining switch which, in accordance with the invention, includes for each half only a single FIFO register, specifically the Queue FIFO, which has an output directly coupled to an output port of the switch.

Referring now to Figure 2 there is shown a forward path of a 2 X 2 combining switch 10 constructed in accordance with the invention, it being realized that the switch includes two halves which are constructed in substantially identical fashion. As such, only the upper half of the switch 10 will be discussed, corresponding structure of the lower half of the switch 10 being indicated with a primed reference numeral. Switch 10 includes two input nodes or ports which are coupled to a two input multiplexer 12 which receives I and J message inputs from data processors (not shown) either directly or through a data concentrator. If the switch 10 is located at one of the inner stages of a log(n) switching network the I and J inputs are coupled to the outputs of a combining switch 10 of a previous stage. Multiplexer 12 directs one of the incoming messages, if there are no contentions or congestions at a switch output node 14, and a Queue FIFO 16 is empty, directly to the output port 14 and eventually to one of a plurality of memory modules (not shown). If the output port 14 is busy and the Queue 16 is empty the incoming message is routed to the Queue FIFO 16 for storage via a two input multiplexer 18. However, if the Queue FIFO 16 is not empty, indicating that other outgoing processor messages are stored therein, at least an address portion and more typically both the address and an operation code portion of the incoming message are first compared by a comparator 20 to corresponding portions of all existing messages stored in the Queue FIFO 16. A determination is thus made if the incoming message is destined for a memory address location which already has a queued message. As was stated, in addition to comparing the address location portion or field of the message the comparator 20 typically also compares the operation type portion or field of the message such that only those messages which are directed to the same memory location and which perform the same type of operation, such as READ, WRITE or FETCH_AND_ADD, are combined. So long as the Queue FIFO 16 is not empty this comparison occurs whether or not the output port 14 is busy. If no match is determined by comparator 20 between the memory address and the operation type associated with the received message and the memory addresses and operation types associated with the queued messages the received message is routed through multiplexer 18 to the Queue FIFO 16 for storage. If comparator 20 determines that the memory address and operation type of the incoming message matches that of a message already stored in the Queue FIFO 16 both the incoming message and the matching queued message are each temporarily stored in an associated register 22 and 24, respectively, for application to a message combining ALU 26. The registered messages are also supplied to a Wait Buffer of an associated message decombining switch (not shown) for later decombination of a message returned from the memory. The ALU 26 generates a combined memory module message which is temporarily stored by ALU output register 28 and which is applied to a second input of multiplexer 18 for storage within the Queue 16. As an example, if both the received message and a queued message indicate a

FETCH_AND_ADD operation at the same memory address, the ADD operand of each message are summed by the ALU 26 to generate a single message to that memory location.

In accordance with one aspect of the invention, the combined message from ALU 26 is stored at the same Queue FIFO 16 location as the existing Queue message which generated a comparison match with the incoming message. Thus, the existing message is over-written and replaced by the combined message. Subsequently the queued messages are extracted from the Queue 16 in a first-in/first-out manner for application to the output port 14 as the output port 14 becomes available for transmission to the memory modules or further stages of the switching network.

The switch 10 also includes a control logic block 30 which is responsive to a comparator 20 output signal and a busy condition of the output port 14 to control the operation, in the manner described above, of the FIFO 16 and the various multiplexers and registers. In addition, the switch 10 includes further logic for determining if the incoming message should be directed to port P or Q. The switch typically also includes logic including protocol signals for communicating with preceding and following 2 X 2 switches.

As can readily be seen the combining switch 10 of the invention eliminates both of the Chute FIFOs 2 of the conventional switch of Fig. 1. This elimination of the Chute FIFOs furthermore eliminates, for example, eight transistors per FIFO storage cell. Assuming a six storage location deep by four word wide FIFO, each word being 32 bits in length, a total of 6,144 transistors are eliminated for the one half of the combining switch or a total of 12,288 transistors for entire combining switch 10. As a result, a significant savings in integrated circuit surface area and combining switch power consumption is achieved.

Furthermore, in that incoming messages are routed through the ALU 26 only if there is a match with a queued message a considerable speed advantage is realized over the conventional combining switch of Fig. 1. That is, the Queue 16 output is coupled directly to the output port 14 multiplexer instead of being coupled to the input of the ALU 26. In the conventional combining switch of Fig. 1 all outgoing messages are sent through the ALU to the output port from the Queue and Chute FIFOs regardless of whether the message requires combination. As such, the conventional combining switch incurs for each output message a propagation delay associated with passage through the ALU.

Claims

1. Digital combining switch apparatus having an input node means (I, J) and an output node means (P, Q), comprising:

storage means (16) having a plurality of storage locations for storing data received from the input node means (I, J) prior to transmission of the data to the output node means (P, Q);

comparator means (20) for comparing the received data to all previously received data, if any, which is stored within the storage means (16), the comparator means (20) having an output for indicating if at least one element of the received data matches at least one element of the stored data; characterized by

combining means (26) having a first input coupled to the received data and a second input coupled to the storage means (16) for combining stored data with the received data, the combining means (26) being responsive to the comparator means (20) output for generating at an output thereof combined data, the combined data being a combination of the received data and the stored data which generated a match with the received data; and

means (30) for directing the combined data from the output of the combining means (26) to the storage means (16) for storage at a location wherein the stored data which generated a match with the received data is stored.

2. Digital combining switch apparatus as set forth in Claim 1 which is included in a data processing system of the type which includes a plurality of data processors which are coupled to a plurality of memory modules through a switching network, the data processors generating messages for storage within a particular one of the memory modules, the input node means (I, J) being coupled to at least one data processor and the output node means (P, Q) being coupled to at least one memory module.

3. Digital combining switch apparatus as set forth in Claim 1 or 2 and further comprising first coupling means (MUX) for coupling an output of the storage means (16) to the output node means (P, Q) for providing stored data thereto.

4. Digital combining switch apparatus as set forth in one of Claims 1 to 3 and further comprising second coupling means (12) for coupling the input node (I, J) means to the output node means (P, Q) if the storage means (16) is empty and if the output node means (P, Q) is available for use.

5. Digital combining switch apparatus as set forth in one of Claims 1 to 4 and further comprising third coupling means (18) for coupling the input node means (I, J) to the storage means (16) for storing the received data at an available storage location within the storage means (16), the third coupling

means (18) being responsive to the comparator means (20) output for coupling the received data from the input node means (I, J) to the storage means (16) when the comparator means (20) output indicates that the at least one element of the received data does not match the at least one element of the stored data.

6. Digital combining switch apparatus as set forth in one of Claims 1 to 5 wherein the received data is expressive of a message generated by one of a plurality of data processors for storage within one of a plurality of memory modules and wherein the at least one element of data is expressive of an identification of a storage location address of one of the memory modules.

7. Digital combining switch apparatus as set forth in one of Claims 1 to 6 wherein the storage means (16) comprises a first-in/first-out storage means.

8. Digital combining switch apparatus as set forth in one of Claims 1 to 7 wherein the combining means (26) comprises an arithmetic/logic unit.

9. Method of operating a message combining switch comprised of a message storage means (16) and an input node means (I, J) coupled to at least one data processor and an output node means (P, Q) coupled to the memory locations, the method comprising the steps of: receiving a message from the input port means (I, J);
characterized by the steps of:
if the message storage means (16) has at least one message stored within,
comparing (20) at least an identification of a memory location and a message operation type associated with the received message to the identification of a memory location and a message operation type associated with messages stored in the message storage means (16);
if at least the memory location and operation type associated with one of the stored messages is determined to be equal to the memory location and operation type associated with the received message,
combining (26) the received message and the stored message to generate a combined message; and
replacing (30) the stored message with the combined message.

10. A method as set forth in Claim 9 and further comprising a step of, when the memory location and/or the operation type associated with each of the stored messages is determined not to be equal to the memory location and/or the operation type associated with the received message, storing the received message at an available storage location within the message storage means (16).

11. A method as set forth in Claim 9 or 10 wherein the step of receiving includes an additional step of, when the message storage means (16) has no messages stored within and when the output port means is available for use, coupling the received message to the output node means (P, Q) for transmission therefrom.

12. A method as set forth in one of Claims 9 to 11 and further comprising a step of transferring messages from the message storage means (16) to the output node means (P, Q) for transmission therefrom, the step of transferring being accomplished such that the first message stored within the message storage means (16) is the first message transferred out of the message storage means (16).

Patentansprüche

1. Digitale Kombinierschalter-Vorrichtung mit Eingangsknoten mitteln (I, J) und Ausgangsknotenmitteln (P, Q), umfassend:
Speichermittel (16), die eine Vielzahl Speicherplätze besitzen, um die Daten, die von den Eingangsknotenmitteln (I, J) empfangen wurden, vor dem Übertragen der Daten zu den Ausgangsknotenmitteln (P, Q) zu speichern;
Komparatormittel (20) zum Vergleichen der empfangenen Daten mit allen vorhergehend empfangenen Daten, welche in den Speichermitteln (16) gespeichert sind, wobei die Komparatormittel (20) einen Ausgang besitzen, der anzeigt, ob mindestens ein Element der empfangenen Daten mit mindestens einem Element der gespeicherten Daten übereinstimmt; gekennzeichnet durch Kombiniermittel (26), die einen ersten Eingang besitzen, der an die empfangenen Daten angeschlossen ist, sowie einen zweiten Eingang, der an die Speichermittel (16) angeschlossen ist, um die gespeicherten Daten mit den empfangenen Daten zu kombinieren, wobei die Kombiniermittel (26) auf das Ausgangssignal der Komparatormittel (26) reagieren, um an einem Ausgang die kombinierten Daten zu erzeugen, wobei die kombinierten Daten eine Kombination der empfangenen Daten und der gespeicherten Daten sind, welche durch eine Übereinstimmung mit den empfangenen Daten erzeugt wird; und
Mittel (30) zum Leiten der kombinierten Daten vom Ausgang der Kombiniermittel (26) zu den Speichermitteln (16); um diese an einem Speicherplatz zu speichern, an dem die gespeicher-

ten Daten, welche eine Übereinstimmung mit den empfangen Daten hervorgerufen haben, gespeichert sind.

2. Digitale Kombinierschalter-Vorrichtung nach Anspruch 1, welche in einem Datenverarbeitungssystem eines Typs enthalten ist, der eine Vielzahl Datenprozessoren enthält, die über ein Vermittlungsnetzwerk mit einer Vielzahl Speichermodule verbunden sind, wobei die Datenprozessoren Nachrichten zum Speichern innerhalb eines speziellen Speichermoduls erzeugen, die Eingangsknotenmittel (I, J) an mindestens einen Datenprozessor angeschlossen sind und die Ausgangsknotenmittel (P, Q) an mindestens ein Speichermodul angeschlossen sind.

3. Digitale Kombinierschalter-Vorrichtung nach Anspruch 1 oder 2, desweiteren erste Kopplungsmittel (MUX) zum Koppeln eines Ausgangs der Speichermittel (16) an die Ausgangsknotenmittel (P, Q) zwecks dortiger Bereitstellung gespeicherter Daten umfassend.

4. Digitale Kombinierschalter-Vorrichtung nach einem der Ansprüche 1 bis 3, desweiteren zweite Kopplungsmittel (12) umfassend, um die Eingangsknotenmittel (I, J) an die Ausgangsknotenmittel (P, Q) anzukoppeln wenn die Speichermittel (16) leer sind und wenn die Ausgangsknotenmittel (P, Q) zur Benutzung verfügbar sind.

5. Digitale Kombinierschalter-Vorrichtung nach einem der Ansprüche 1 bis 4, desweiteren dritte Kopplungsmittel (18) umfassend, um die Eingangsknotenmittel (I, J) zum Speichern der empfangenen Daten auf verfügbaren Speicherplätzen innerhalb der Speichermittel (16) an die Speichermittel (16) anzukoppeln, wobei die dritten Kopplungsmittel auf das Ausgangssignal der Komparatormittel (20) reagieren, um die empfangenen Daten von den Eingangsknotenmitteln (I, J) auf die Speichermittel (16) zu schalten, wenn die Komparatormittel (20) anzeigen, daß das mindestens eine Element der empfangenen Daten nicht mit dem mindestens einen Element der gespeicherten Daten übereinstimmt.

6. Digitale Kombinierschalter-Vorrichtung nach einem der Ansprüche 1 bis 5, wobei die empfangenen Daten Ausdruck für eine Nachricht sind, die durch einen aus der Vielzahl der Datenprozessoren zur Speicherung innerhalb eines aus der Vielzahl der Speichermodule erzeugt wurde und wobei das mindestens eine Element der Daten ein Ausdruck für die Identifikation der Speicherplatzadresse eines der Speichermodule ist.

7. Digitale Kombinierschalter-Vorrichtung nach einem der Ansprüche 1 bis 6, wobei die Speichermittel (16) FIFO-Speichermittel umfassen.

8. Digitale Kombinierschalter-Vorrichtung nach einem der Ansprüche 1 bis 7, wobei die Kombiniermittel (26) eine Arithmetik-Logik-Einheit umfassen.

9. Verfahren zum Betrieb eines Nachrichten-Kombinierschalters, Speichermittel (16) und Eingangsknotenmittel (I, J), die an mindestens einen Datenprozessor angeschlossen sind, und Ausgangsknotenmittel (P, Q), die an Speicherplätze angeschlossen sind, umfassend, wobei das Verfahren die folgenden Schritte umfaßt:
Empfangen einer Nachricht von den Eingangsportmitteln (I, J)
gekennzeichnet durch die Schritte:
wenn in den Nachrichten-Speichermitteln (16) mindestens eine Nachricht gespeichert ist,
Vergleichen (20) von mindestens einem Identifikationsmerkmal des Speicherplatzes und des Nachrichten-Operationstyps, die der empfangenen Nachricht zugeordnet sind, mit dem Identifikationsmerkmal eines Speicherplatzes und einem Nachrichten-Operationstyp, die Nachrichten zugeordnet sind, welche in den Nachrichten-Speichermitteln (16) gespeichert sind;
wenn festgestellt wird, daß mindestens der Speicherplatz und der Operationstyp, die einer der gespeicherten Nachrichten zugeordnet sind, dem Speicherplatz und dem Operationstyp entsprechen, die der empfangenen Nachricht zugeordnet sind,
Kombinieren (26) der empfangenen Nachricht und der gespeicherten Nachricht, um eine kombinierte Nachricht zu erzeugen; und
Ersetzen (30) der gespeicherten Nachricht durch die kombinierte Nachricht.

10. Verfahren nach Anspruch 9, desweiteren einen Schritt umfassend, bei dem, wenn festgestellt wird, daß die Speicherplätze und/oder Operationstypen, die jeder gespeicherten Nachricht zugeordnet sind, nicht dem Speicherplatz und/oder Operationstyp, die der empfangenen Nachricht zugeordnet sind, entsprechen, die empfangene Nachricht auf einem verfügbaren Speicherplatz in den Nachrichten-Speichermitteln (16) gespeichert wird.

11. Verfahren nach Anspruch 9 oder 10, wobei der Schritt des Empfangens einen zusätzlichen Schritt umfaßt, bei dem, wenn in den Nachrichten-Speichermitteln (16) keine Nachrichten gespeichert sind und wenn die Ausgangsportmittel zur Benutzung verfügbar sind, die empfangene

Nachricht auf die Ausgangsknotenmittel (P, Q) geschaltet wird, um von diesen weitergesendet zu werden.

12. Verfahren nach einem der Ansprüche 9 bis 11, desweiteren den Schritt des Übertragens von Nachrichten von den Nachrichten-Speichermitteln (16) zu den Ausgangsknotenmitteln (P, Q) umfassend, von denen die Nachrichten dann weitergesendet werden, wobei der Übertragungsschritt so ausgeführt wird, daß die zuerst in den Nachrichten-Speichermitteln (16) gespeicherte Nachricht auch die erste Nachricht ist, die aus den Nachrichten-Speichermitteln ausgegeben wird.

Revendications

1. Dispositif de commutateur numérique par combinaison comportant un moyen de noeud d'entrée (I, J) et un moyen de noeud de sortie (P, Q), comprenant :
des moyens de stockage (16) comportant une pluralité d'emplacements de stockage pour stocker les données reçues du moyen de noeud d'entrée (I, J) avant la transmission des données au moyen de noeud de sortie (P, Q),
des moyens de comparateur (20) pour comparer les données reçues à la totalité des données reçues précédemment, s'il y en a, qui sont stockées dans les moyens de stockage (16), les moyens de comparateur (20) comportant une sortie pour indiquer si au moins un élément des données reçues concorde avec au moins un élément des données stockées, caractérisé par
des moyens de combinaison (26) comportant une première entrée couplée aux données reçues et une seconde entrée couplée aux moyens de stockage (16) pour combiner les données stockées avec les données reçues, les moyens de combinaison (26) répondant à la sortie des moyens de comparateur (20) pour produire à leur sortie les données combinées, les données combinées constituant une combinaison des données reçues et des données stockées qui ont produit une concordance avec les données reçues, et
des moyens (30) pour diriger les données combinées provenant de la sortie des moyens de combinaison (26) vers les moyens de stockage (16) pour stockage à un emplacement dans lequel les données stockées qui ont produit une concordance avec les données reçues sont stockées.

2. Dispositif de commutateur numérique par combinaison selon la revendication 1, qui est inclus dans un système de traitement de données du type qui comporte une pluralité de processeurs de données qui sont couplés à une pluralité de modules mémoires par l'intermédiaire d'un réseau de commutation, les processeurs de données produisant des messages pour stockage à l'intérieur d'un module particulier parmi les modules mémoires, les moyens de noeud d'entrée (I, J) étant couplés à au moins un processeur de données et les moyens de noeud de sortie (P, Q) étant couplés à au moins un module mémoire.

3. Dispositif de commutateur numérique par combinaison selon la revendication 1 ou 2, et comprenant de plus des premiers moyens de couplage (MUX) pour coupler une sortie des moyens de stockage (16) aux moyens de noeud de sortie (P, Q) pour délivrer des données stockées à ceux-ci.

4. Dispositif de commutateur numérique par combinaison selon l'une quelconque des revendications 1 à 3 et comprenant de plus des seconds moyens de couplage (12) pour coupler les moyens de noeud d'entrée (I, J) aux moyens de noeud de sortie (P, Q) si les moyens de stockage (16) sont vides et si les moyens de noeud de sortie (P, Q) sont disponibles pour utilisation.

5. Dispositif de commutateur numérique par combinaison selon l'une quelconque des revendications 1 à 4 et comprenant de plus des troisièmes moyens de couplage (18) pour coupler les moyens de noeud d'entrée (I, J) aux moyens de stockage (16) pour stocker les données reçues à un emplacement de stockage disponible parmi les moyens de stockage (16), les troisièmes moyens de couplage (18) répondant à la sortie des moyens de comparateur (20) pour coupler les données reçues provenant des moyens de noeud d'entrée (I, J) aux moyens de stockage (16) lorsque la sortie des moyens de comparateur (20) indique qu'au moins un élément des données reçues ne concorde pas avec au moins un élément des données stockées.

6. Dispositif de commutateur numérique par combinaison selon l'une quelconque des revendications 1 à 5, dans lequel les données reçues sont représentatives d'un message produit par l'un d'une pluralité de processeurs de données pour stockage à l'intérieur de l'un d'une pluralité de modules mémoires dans lequel le au moins un élément de données est représentatif d'une identification d'une adresse d'emplacement de stockage de l'un des modules mémoires.

7. Dispositif de commutateur numérique par combinaison selon l'une quelconque des revendica-

tions 1 à 6, dans lequel les moyens de stockage (16) comprennent des moyens de stockage du type premier entré/premier sorti.

8. Dispositif de commutateur numérique par combinaison selon l'une quelconque des revendications 1 à 7, dans lequel les moyens de combinaison (26) comprennent une unité arithmétique/logique.

9. Procédé pour mettre en oeuvre un commutateur à combinaison de message constitué de moyens de stockage de message (16) et d'un moyen de noeud d'entrée (I, J) couplé à au moins un processeur de données, et d'un moyen de noeud de sortie (P, Q) couplé aux emplacements mémoires, le procédé comprenant les étapes consistant à :
recevoir un message du moyen d'accès d'entrée (I, J),
caractérisé par les étapes consistant à :
si le moyen de stockage de message (16) comporte au moins un message stocké dans celui-ci,
comparer (20) au moins une identification d'un emplacement mémoire et un type d'opération de message associé au message reçu à l'identification d'un emplacement mémoire et à un type d'opération de message associé au message stocké dans les moyens de stockage de message (16),
si au moins l'emplacement mémoire et le type d'opération associé à l'un des messages stockés sont déterminés être égaux à l'emplacement mémoire et au type d'opération associé au message reçu,
combiner (26) le message reçu et le message stocké afin de produire un message combiné, et remplacer (30) le message stocké par le message combiné.

10. Procédé selon la revendication 9 et comprenant de plus une étape consistant à, lorsque l'emplacement mémoire et/ou le type d'opération associé à chacun des messages stockés sont déterminés ne pas être égaux à l'emplacement mémoire et/ou au type d'opération associé au message reçu, stocker le message reçu à un emplacement mémoire disponible dans les moyens de stockage de message (16).

11. Procédé selon la revendication 9 ou 10, dans lequel l'étape de réception comporte une étape supplémentaire consistant à, lorsque le moyen de stockage de message (16) ne comporte pas de message stocké et lorsque le moyen d'accès de sortie est disponible pour utilisation, coupler le message reçu aux moyens de noeud de sortie (P, Q) pour transmission à partir de celui-ci.

12. Procédé selon l'une quelconque des revendications 9 à 11 et comprenant de plus une étape consistant à transférer le message à partir des moyens de stockage de message (16) aux moyens de noeud de sortie (P, Q) pour transmission à partir de ceux-ci, l'étape de transfert étant accomplie de telle sorte que le premier message stocké dans les moyens de stockage de message (16) soit le premier message transféré hors des moyens de stockage de message (16).

FIG.1 (PRIOR ART)

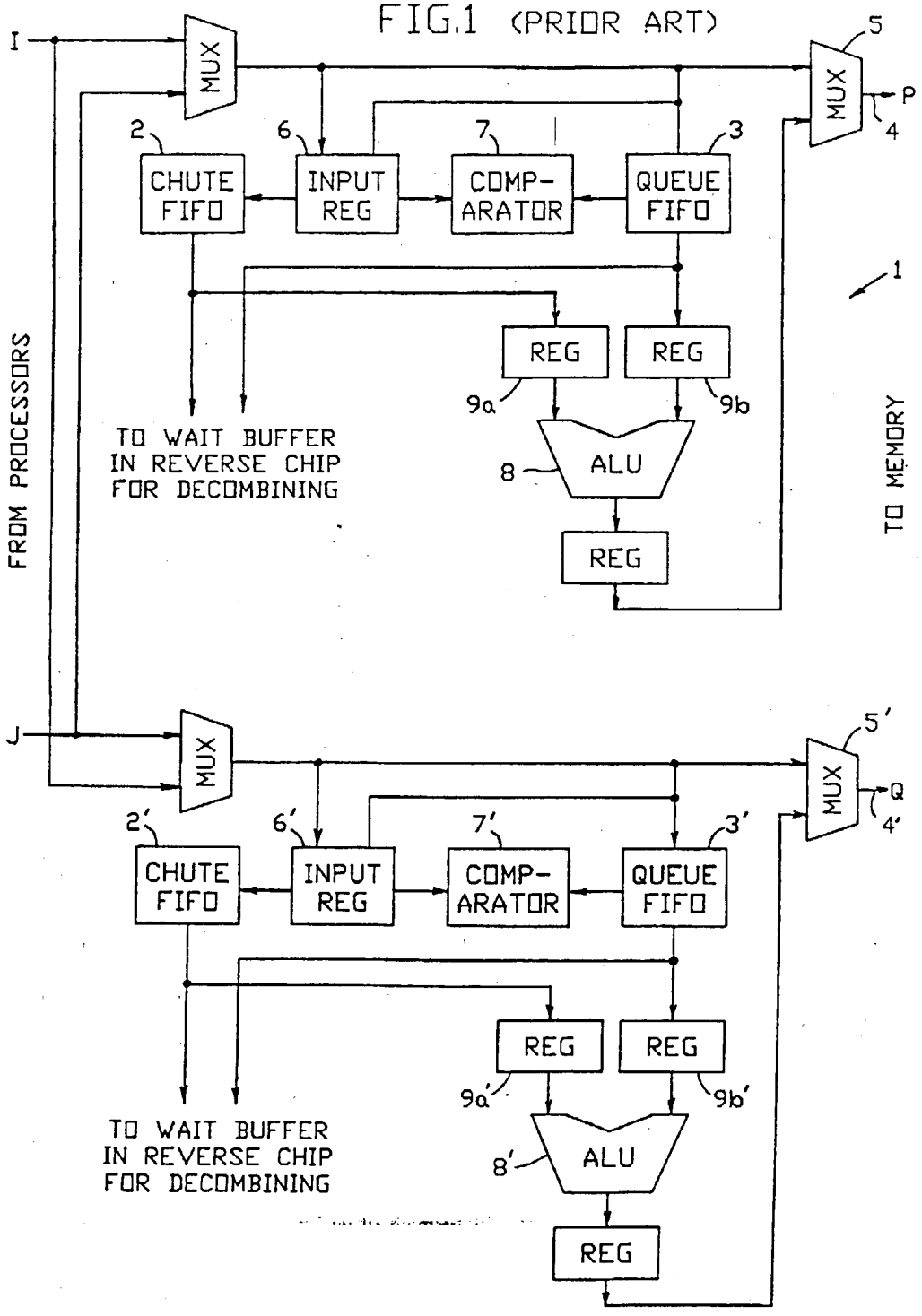
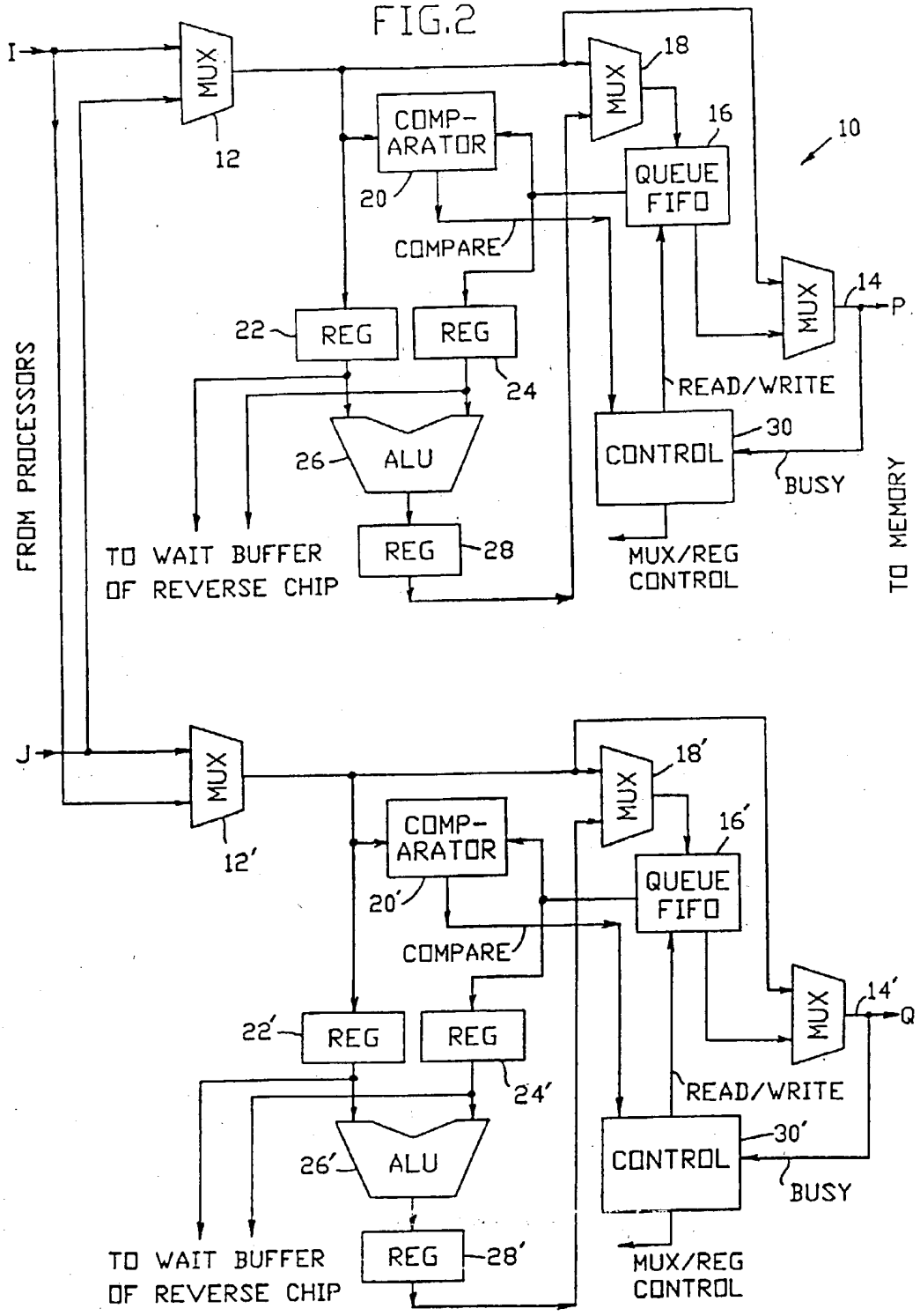


FIG.2


I
MUX
12
COMP-
ARATOR
20
COMPARE
MUX
18
16
QUEUE
FIFO
10
MUX
14
P
22
REG
REG
24
READ/WRITE
26
ALU
CONTROL
30
BUSY
FROM PROCESSORS
TO WAIT BUFFER
OF REVERSE CHIP
REG
28
MUX/REG
CONTROL
TO MEMORY
J
MUX
12'
COMP-
ARATOR
20'
COMPARE
MUX
18'
16'
QUEUE
FIFO
MUX
14'
Q
22'
REG
REG
24'
READ/WRITE
26'
ALU
CONTROL
30'
BUSY
TO WAIT BUFFER
OF REVERSE CHIP
REG
28'
MUX/REG
CONTROL